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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,175	09/28/2000	Victor Konrad	042390.P9573	2921

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,175	KONRAD ET AL.	
	Examin r	Art Unit	
	Helen B Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-19 and 22-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-19 and 22-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 09/678,175 filed 09/28/2000 and amendment filed 01/26/2004.

2. Claims 1-3, 6-19 and 22-40 remain pending in the Application.

3. Applicant's arguments have been fully considered. Examiner does not find them persuasive.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 10, 12-14, 24 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Katkoori et al. ("Simulation based architectural power estimation for PLA-based controllers ").

As to claims 10 and 24 Katkoori et al. teaches determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) by specifying the number of output variables (|O|), the number of input variables (|I|) and the number of terms (|T|) for synthesizing a PLA using a set of Boolean equations (Page 122); dividing the set of equations representing the PLA into equations representing a plurality of sub-PLAs as shown on the Fig. 1 representing the PLA block as a set of sub-components (Page 122); merging outputs of the equations representing the plurality of sub-PLAs as shown as a part of the fragment of VHDL code (Page 123); determining a

topological circuit representation of the equations representing the plurality of sub-PLAs as shown on the Fig. 1; applying gating logic to the topological circuit representation of the plurality of sub-PLAs within a typical PLA which is implemented as AND-OR structure which is logic of gates; controlling power consumption in the topological representation of the plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes to power consumption within the modeling of power consumption due to node activity in AND plane and OR plane is more involved (Page 123).

As to claims 12-14 and 26 Katkoori et al. teaches the equations representing the plurality of sub-PLAs are divided recursively based on a determined optimum splitting variable for each equation representing a sub-PLA wherein the power characterization involves extracting equations for different sub-components of PLAs (abstract); each product of the equations representing the plurality of sub-PLAs is obtained by omitting literals in the equations representing the PLA; a product of the omitted literals is used in the topological circuit representation of the plurality of sub-PLAs to gate a clock of each product of the plurality of sub-PLAs to gate a clock of each product of the plurality of sub-PLAs within the minimization of equations obtained after the logic minimization (Page 123).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 6-9, 17-19, 22, 23, 29-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ditlow et al. (US Patent 5,311,079) in view of Shau (US Patent 6,492,835).

As to claims 1-3, 6-9, 17-19, 22, 23, 29-40 Ditlow et al. teaches determining an optimum splitting variable as input lines x_1, x_2 and x_3 input Boolean variables and y_1 and y_2 as output Boolean variables (col. 3, ll.44-46; ll.52-54; Fig. 9); dividing a set of equations representing a programmable logic array (PLA) into a first set of equations representing a first sub-PLA and a second set of equations representing a second sub-PLA based on splitting variables (Fig. 8); determining a topological circuit representation of the equations by presenting the Fig. 2 and Fig. 3 wherein the Fig. 2 represents a first sub-PLA and Fig. 3 represents a second sub-PLA (col. 4, ll.1-6); applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA as shown in the equations (col.5, ll.60-67; col. 6, ll.1-29; col. 8, ll.34-38); and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption using the selective activation approach to activate the pullup devices (col. 2, ll.65-68; col. 3, ll.1-4; ll.8-12). Moreover Ditlow et al. teaches merging an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA, wherein merging the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA forms a logical equivalent of the PLA as

shown on the Fig. 9 which is represents the PLA/decoder and divided portion of it shown on the Fig. 2 and Fig. 3 (col. 4, ll.57-62); the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented as shown on the Fig. 2 the output lines y_1 and y_2 and product terms lines PT1-PT4 are realized in the table on the Fig. 9 and the output lines (DD, TD, CD, CC, DC) as shown on the Fig. 3 can be activated according the input lines x_2 and x_3 (col. 4, ll.35-40); delaying a clock to an OR plane of one of the topological circuit representation of the first sub-PLA and the topological circuit representation of the second sub-PLA (col. 2, ll.14-18); determining the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA as shown on the Fig. 10 (col. 6, 48-54). However Ditlow et al. lacks the specifics regarding computer aided design and the layout and arrangements of OR plane in the PLA. Shau teaches the PLA to be divided is partially optimized by computer aided design (CAD) (col. 1, ll.20-25); an OR plane of the topological circuit representation of the first sub-PLA is interleaved with an OR plane of the topological circuit representation of the second sub-PLA; an OR plane of the topological circuit representation of the first sub-PLA is separated from an OR plane of the topological circuit representation of the second sub-PLA as shown on the Fig. 3(c) wherein (331) and (332) are first sub-PLA and second sub-PLA respectively, (381) is a OR array of the first sub-PLA, (382) is OR array of the second

sub-PLA and they are separated and interleaved using domino circuits for connection between sub-PLA's and their elements (OR arrays) (col. 8, ll.45-47; col. 10, ll.11-14); determining a topological circuit representation of first sub-PLA and the second sub-PLA is created by computer aided design (abstract; col. 1, ll.20-25). It would have been obvious to one of ordinary skill on the art at the time the invention was made to have used Shau to teach the specifics subject matter Ditlow et al. does not teach, because a large PLA is divided into smaller sub-PLA while individual sub-PLA's are controlled separately which makes it possible to save power with better performance and better cost efficiency (abstract).

8. Claims 11 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katkoori et al. as applied to claims 10 and 24 above, and further in view of Shau.

As to claims 11 and 25 Katkoori et al. teaches the limitations from which the claims depend. However Katkoori et al. lacks specifics regarding computer-aided design. Shau teaches the PLA to be divided is partially optimized by computer aided design (CAD) (col. 1, ll.20-25). It would have been obvious to one of ordinary skill on the art at the time the invention was made to have used Shau to teach the specifics subject matter Katkoori et al. does not teach, because a large PLA is divided into smaller sub-PLA while individual sub-PLA's are controlled separately which makes it possible to save power with better performance and better cost efficiency (abstract).

9. Claims 15, 16, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katkoori et al. as applied to claims 10, 12, 24 and 26 above, and further in view of Ditlow et al.

As to claims 15, 16, 27 and 28 Katkoori et al. teaches the limitations from which the claims depend. However Katkoori et al. lacks specifics regarding AND plane. Ditlow et al. teaches determining the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the equations representing the PLA as shown on the Fig. 7 wherein "select" column shows activated output lines for a given inputs (x_2, x_3) and avoiding the state of the input signal which is marked as dash (don't care or unbalanced signal) (col. 4, ll.38-46); selecting a column with smallest overhead in the AND plane of the equations representing the PLA as shown on the Fig. 10, wherein the smallest value ("1" vs. "2") gives a better result of power consumption as a result of the calculations demonstrated by the equations (in the columns 5 and 6), which are PT_3 and PT_4 (product terms) and more desirable (col. 5, ll.43-46; col. 6, 48-54). It would have been obvious to one of ordinary skill on the art at the time the invention was made to have used Ditlow et al. to teach the specifics subject matter Katkoori et al. does not teach, because it makes possible to activate the pullup devices associated with the product terms selectively, based upon decoding and selective activation approach, which provides a significantly greater reduction in the power consumption (col. 2, ll.65-67; col. 3, ll.1-3).

Remarks

10. Applicant's arguments only recite the claim limitations and assert without evidence that Applicant's claims limitations distinguish over Katkoori's reference. Applicant's limitations of the Claim 10 and 24 do not distinguish over Katkoori. Katkoori discloses splitting a PLA into sub-PLAs as shown on the Fig. 1 wherein the block

diagram identifies four sub-components such as AND plane, OR plane, Input Buffer and Output buffer (page 122) and considering an input column in a PLA with six product terms as shown on the Fig. 2, wherein the input variable x appears in two product terms and its complement appears in three product terms having an event from 0 to 1 on the input line and similar to the input column, an output column has nodes in the OR plane with each node selecting a term, wherein to ensure terms a set of simple irredundant Boolean equations is generated; the terms so selected are combined to form the output line (optimum splitting variable) since event from 1 to 0 on x line implies events from 1 to 0 at the output line; this is obtained from the optimized equations (page 123).

Turning now to the rejection *35 USC § 103,* Applicant asserts that there is no motivation to combine Ditlow and Shau, Ditlow teaches optimum variables (x1, x2 and x3 and y1 and y2) carrying the input signals and output signals to implement a product term lines PT1-PT4 as Boolean function (col. 3, ll.44046; ll.64-65) and dividing the PLA into plurality of sub-PLAs as shown on the Fig. 2 and Fig. 3 wherein PLA has been divided shown on the Fig. 1 and Shau teaches the specifics regarding computer aided design and the layout and arrangements of OR plane in the PLA Ditlow does not teach; so the combination of Ditlow and Shau teaches all limitations of claims 2, 3, 6-9, 18, 19, 22 and 23. Based on these disclosures in Ditlow and Shau the rejection under *35 USC § 103 i*s maintained.

Now having the combination of Katkoori and Shau teaches all limitations of claims 11 and 25 since Katkoori teaches the limitation of claims 10 and 24(above), and

claims 11 and 25 depend on them; and Shau teaches the specifics regarding computer aided design Katkoori does not teach.

Moreover the limitations of claims 15,16 and 27 and 28 are taught by the combination of Katkoori because this reference teaches the limitations of claims from which the claims depend (10, 12, 24 and 26) (see above) and Ditlow teaches specifics regarding AND plane Katkoori lacked.

Based on these disclosures Katkoori and Shau the rejection under *35 USC § 103* is maintained.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen B Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HR